IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 1, after the title, is amended as follows:

This application is a divisional of U.S. Patent Application Serial No. 10/025,030, filed December 19, 2001, <u>now issued as U.S. Patent Application Serial No. 6,605,874,</u> which is incorporated herein by reference.

The paragraph beginning at page 1, line 22, is amended as follows:

Copper has recently been introduced as an interconnect material. But copper has technical challenges such as poor adherence to dielectrics and the resulting electromigration by the copper material during device use. Another problem for copper is poor recess fill properties that result in voids. Additionally, [[of]] copper may blister or form hillocks during thermal processing.

The paragraph beginning at page 5, line 13, is amended as follows:

Figures 1A and 1B depict an interconnect zone 120 that defines a surface area for electrical connection. First interconnect 112 is disposed in a dual-damascene recess that may be formed by a two-step etch that first opens a smaller recess by an anisotropic etch, and that second opens a larger recess but that also extends the first, smaller recess to create interconnect zone 120. For example, a via and trench recess is formed by initially using a mask, such as a photoresist mask to define an area for a via opening, and by etching the via with a suitable chemistry, such as, for example, a CH_3/CF_4 or C_4F_8 etch chemistry for <u>an</u> [[a]] SiC dielectric material. The photoresist mask may then be removed such as by an oxygen plasma to remove a photoresist, and a second mask may be patterned to define a greater area for a trench opening. A

subsequent mask and etch is introduced to form a trench and the second mask is removed leaving the substrate shown in Figures 1A and 1B.

The paragraph beginning at page 5, line 24, is amended as follows:

The dual-damascene recess includes a via 122 and a trench 124. Other etch techniques for forming a recess are set forth herein. In any event, first interconnect 112 is disposed in a first recess 122, 124 that is made in a first ILD layer 126, and upper interconnect 116 (Figure 1A) and 117 (Figure 1B) are disposed in an upper recess that includes a via 128 and a trench 130, and that is formed in an upper ILD layer 132. The ILD layer(s) are made of a dielectric material known in the art. For example, it may be silicon dioxide (SiO_2) that is formed by the decomposition <u>of</u> a tetraethylortho silicate (TEOS) or a plasma enhanced chemical vapor deposition (PECVD) source. The dielectric material may also be a material having a dielectric constant less than the dielectric constant of SiO_2 including polymers as known in the art.

The paragraph beginning at page 10, line 9, is amended as follows:

Reducing agents are provided to assist in assuring metal deposition as the chemical environment of the substrate onto which the metal deposits <u>continue</u> ~~continues~~ to change. Although initial deposition of a primary metal onto a substrate may be autocatalytic, the changing chemical environment may interrupt the autocatalytic environment. In one embodiment, where deposition is upon a copper metal-six (Cu M6) pad as known in the art, initial deposition will be achieved in the presence of the Cu M6 pad. Consequently, the copper pad substrate affects the initial, presumably oxidation-reduction (REDOX) deposition chemistry. However, as the Cu M6 pad is covered by way of non-limiting example, by cobalt, the REDOX chemical environment changes from a cobalt-onto-copper plating, to a cobalt-onto-cobalt plating. Accordingly, a reducing agent(s) is provided to assure continued cobalt plating despite the changed substrate environment.

The paragraph beginning at page 15, line 22, is amended as follows:

In another embodiment, cobalt is a primary metal for an electroless plating embodiment, the composition includes a cobalt solution to form a cobalt plating layer. According to an embodiment, where cobalt is the primary metal, because of the inventive electroless plating bath environment, metallic films form that include but are not limited by such combinations as CoB, CoBP, CoCrB, CoCrBP, CoMoB, CoMoBP, CoWB, CoWBP, CoMnB, CoMnBP, CoTcB, CoTcBP, CoReB, and CoReBP. Where two primary metals are used in solution, the inventive electroless plating bath environment may form metallic films that include but <u>are</u> not [[are]] limited by such combinations as to NiCoB, CoPdBP, CoPdCrB, CoPdCrBP, CoPdMoB, CoPdMoBP, CoPdWB, CoPdWBP, CoPdMnB, CoPdMnBP, CoPdTcB, CoPdTcBP, CoPdReB, and CoPdReBP.

The paragraph beginning at page 16, line 14, is amended as follows:

Where, by way of non-limiting example, copper is a primary metal for an electroless plating embodiment. The composition includes a copper solution to form a copper plating layer. According to an embodiment, where copper is the primary metal, because of the inventive electroless plating bath environment, metallic films form that include but are not limited by such combinations as CuB, CuBP, CuCrB, CuCrBP, CuMoB, CuMoBP, CuWB, CuWBP, CuMnB, CuMnBP, CuTcB, CuTcBP, CuReB, and CuReBP. Where two primary metals are used in solution, the inventive electroless plating bath environment may form metallic films that include but <u>are</u> not [[are]] limited by such combinations as to CuNiB, CuNiBP, CuNiCrB, CuNiCrBP, CuNiMoB, CuNiMoBP, CuNiWB, CuNiWBP, CuNiMnB, CuNiMnBP, CuNiTcB, CuNiTcBP, CuNiReB, and CuNiReBP. It can be seen that at least two- to nine primary metals and from zero to at least one secondary metal is combinable according to various embodiments. In similar embodiments, silver can be used in place of- or in addition to copper. Similarly, gold can be used in place of- or in addition to copper. Additionally, a blend of at least two of copper, silver, and gold can be used as set forth herein.

The paragraph beginning at page 17, line 5, is amended as follows:

Referring again to Figures 1A and 1B, the metal of first interconnect 112 and upper interconnects 116 and 117 may be treated to improve the uniformity of the electroless plating of the conductive diffusion barrier materials. Surface treating is done with a [[an]] treatment compound such as a mineral acid. For example, a 1 to 20 volume percent hydrofluoric acid (HF) may be used. Other solutions include, sulfuric acid (H_2S0_4), sulfonic acids such as methanesulfonic acid (MSA), ethanesulfonic acid (ESA), propanesulfonic acid (PSA), benzene sulfonic acid (BSA), and the like.

The paragraph beginning at page 19, line 20, is amended as follows:

Figures 3A and 3B illustrate another embodiment in which disparate types of ILD layers are combined. In Figures 3A and 3B, first ILD layer 326 is an organic material such as a polyimide layer that is formed by spin-on and cure techniques. Other organic types include SiLK® and the like. Other organic types include FLARE® and the like made by Allied Signal of Morristown, New Jersey. Surmounting first ILD layer 326 is a first hard mask 340 that is typically a [[an]] nitride material such as silicon nitride, titanium nitride, tungsten nitride, and the like. Above first hard mask 340 is an inorganic ILD layer (referred to hereinafter as upper ILD layer) 342. It is notable that no upper hard mask is present. First hard mask 340 acts to protect the organic first ILD layer 326 from subsequent processing. The additional ILD layer 138 in this embodiment, is also an organic material and an additional hard mask 339 is provided.

The paragraph beginning at page 23, line 4, is amended as follows:

It can now be appreciated that where "upper" is used in this disclosure, it may mean a [[an]] third architecture, a fourth, a fifth, a sixth, etc. according to the various levels of metallization according to known metallization architectures. Additionally, where a "first" architecture is depicted, it may be an architecture that has other architectures disposed below it. For example referring to Figure 1A, first interconnect 112 may be a metal-five (M5) interconnect, and upper interconnect may be an M6 interconnect.

The paragraph beginning at page 8, beginning a line 16 is amended as follows.

The first conductive diffusion barrier layer 114 and the upper conductive diffusion barrier layer 118 ~~116~~ (Figure 1A) and 119 (Figure 1B) are also formed in order to contain the copper or copper-based interconnects 112, 116, and 117. Various methods for obtaining conductive barrier layer 112, 118 ~~116~~, and 119 ~~117~~ are used according to embodiments. For example, the conductive barrier layers 112, 118 ~~116~~, and 119 ~~117~~ are formed from vapor deposition processing including CVD, plasma-enhanced CVD (PECVD), atomic layer CVD (ALCVD), and PVD.